16. GDP-32^{II} DESIGN

16.1 BASIC DESIGN CHARACTERISTICS 2

16.2 RECEIVER LAYOUT 4

16.3 CARD-PC MPU BOARD 8

16.4 BD287 FRONT PANEL BOARD 8

16.5 BD183 ANALOG BOARD 10

RELAY FUNCTIONS 10
DIFFERENTIAL AMPLIFIER 10
THE OFFSET DAC 10
POWERLINE NOTCH FILTER 13
GAIN STAGES 13
ANTI-ALIAS FILTER 13
MULTIPLEXER 13
ANALOG-TO-DIGITAL CONVERTER 14

16.6 THE CALIBRATION AND TIMING BOARD 18

THE CALIBRATE SECTION AND MULTIPLEXER 18
OHMMETER 18
TIMING SECTION 19

16.7 THE BATTERY COMPARTMENT 23

SMALL CASE DESIGN (GDP-32^{II}T) 23
LARGE CASE DESIGN 23

16.8 THE CRYSTAL OSCILLATOR 23

16.1 BASIC DESIGN CHARACTERISTICS

A complete description of the external characteristics of the GDP-32II is located in **Section 2 – Description of the GDP-32II Receiver**.

The GDP-32II case is divided into two sections: Analog and Digital. These sections are kept separate to minimize noise pickup and for ease in trouble-shooting and repair.

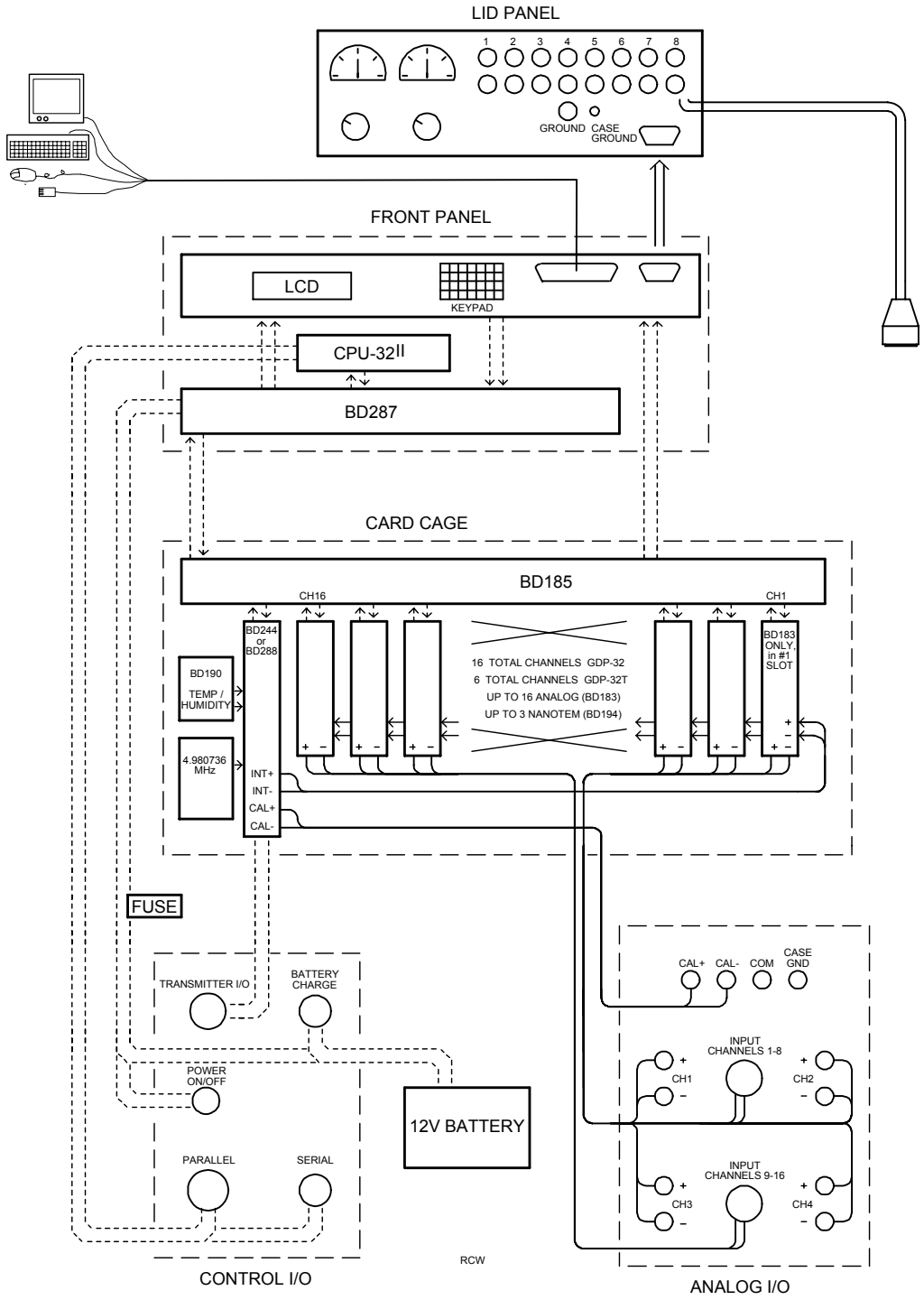

Figure 16.1 (a) - GDP-32II Block Diagram 1

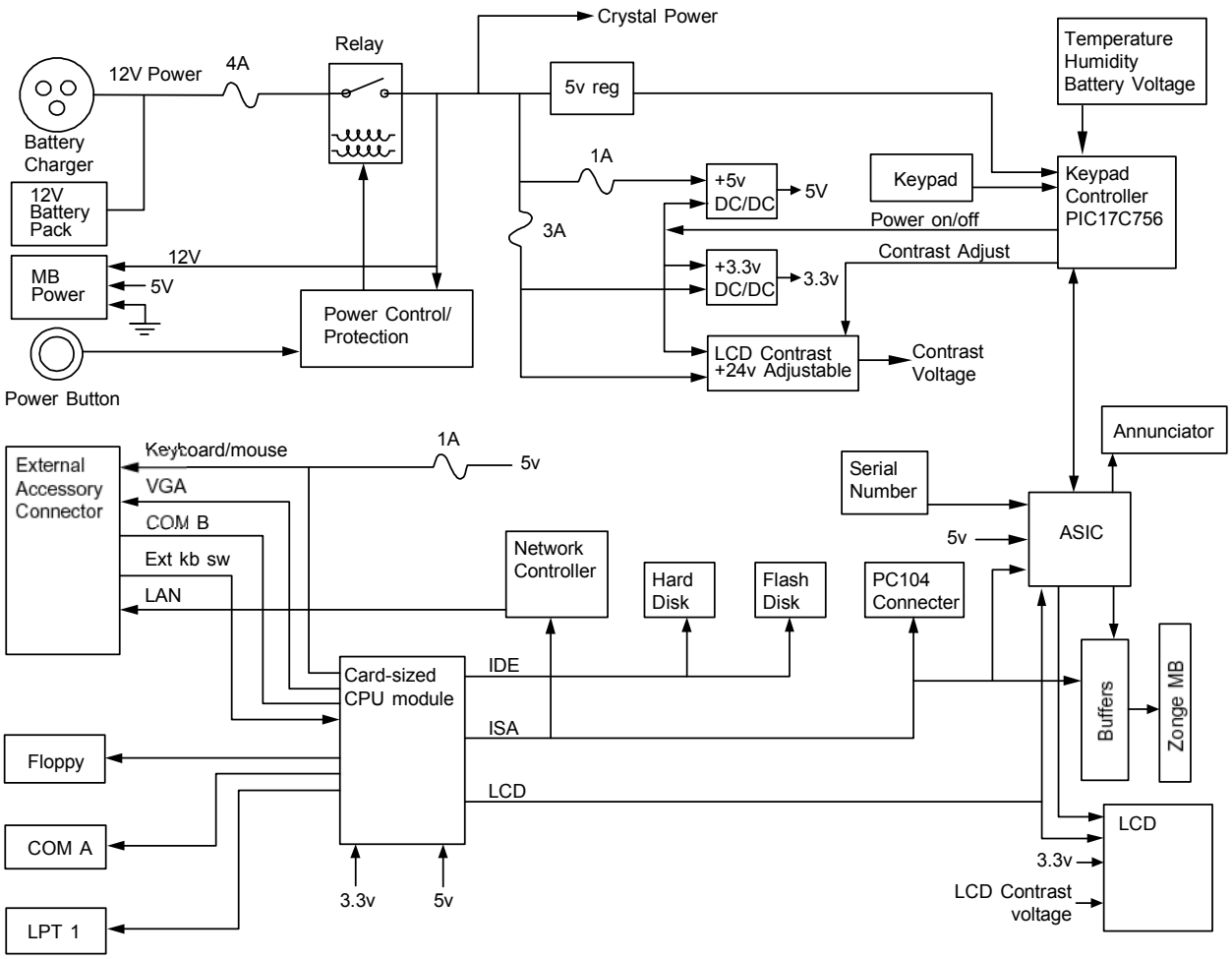

Figure 16.1 (b) - GDP-32^{II} Block Diagram 2

16.2 RECEIVER LAYOUT

Figures 16.1 (a) and (b) are detailed block diagrams of the general layout of the receiver. The package design separates the digital control circuit boards mounted to the front panel from the analog acquisition cards and the timing and calibration card that are inserted into the card cage.

The analog system of the GDP-32^{II} is comprised of the Analog I/O Panel through which signals are connected to as many as 16 analog boards. The analog boards provide necessary gain and filtering prior to A/D conversion. They are mounted in the card cage together with the timing and calibration card.

Each analog card contains:

- Individual power supply
- High-speed sample and hold circuit
- Analog to Digital converter (ADC)

The timing and calibration card contains:

- Counter chains that generate the binary detection frequencies selectable through the program menus.
- Digital to Analog converter (DAC) for generating precision analog test signals for calibration purposes.
- GPS synchronizing Circuitry (BD 288)

The ribbon cables, located between the front panel and the lid, route the amplified and filtered analog signals from each of the analog boards to the panel meter switch.

An oven-stabilized 4.980736 MHz crystal oscillator is mounted directly to the timing board (BD244 or BD288) in the large case GDP-32^{II}. In the small case GDP-32^{II}, the crystal is mounted next to the battery compartment.

Basic control and monitoring of the receiver function is handled by the keyboard and the Front Panel LCD display. Mounted to the underside of the panel is a 66 MHz 586 Card-PC single board computer together with a motherboard (BD287). The front panel assembly consists of the Front Panel, the MPU board and BD287 and constitutes the complete system for digital control of analog data acquisition.

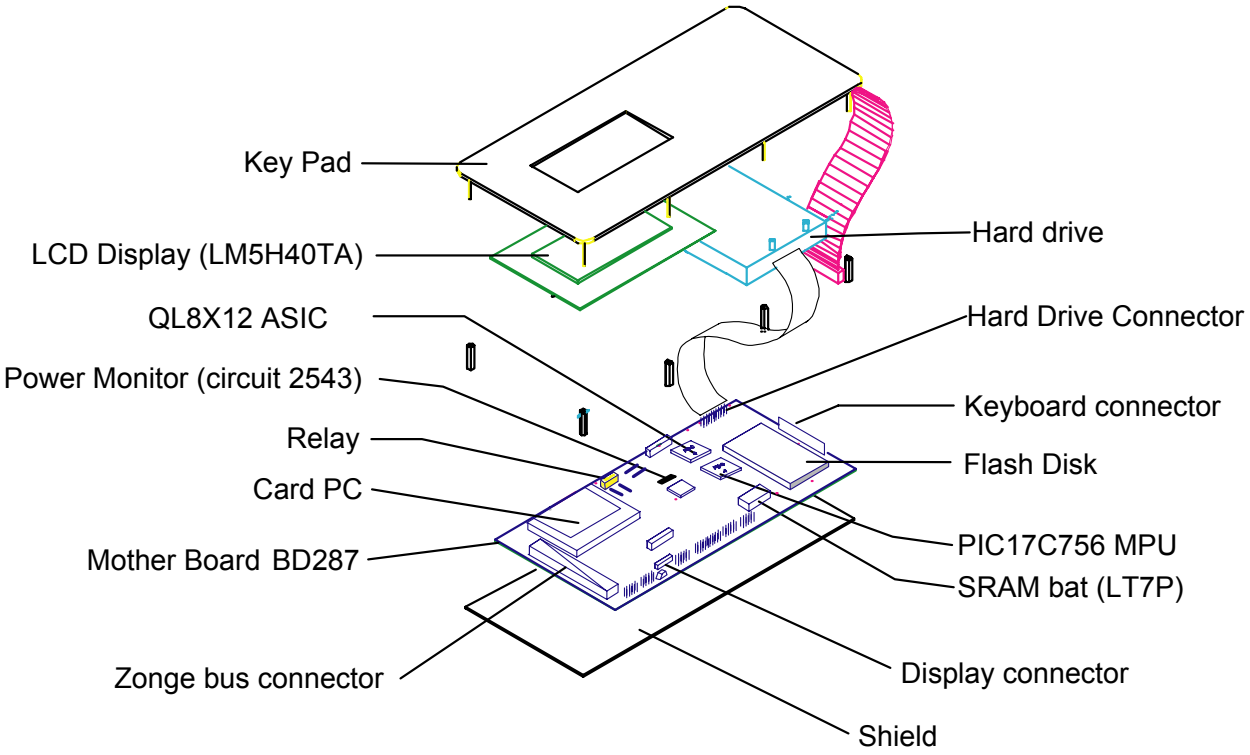

Figure 16.2(a) - Explosion of Front Panel Assembly

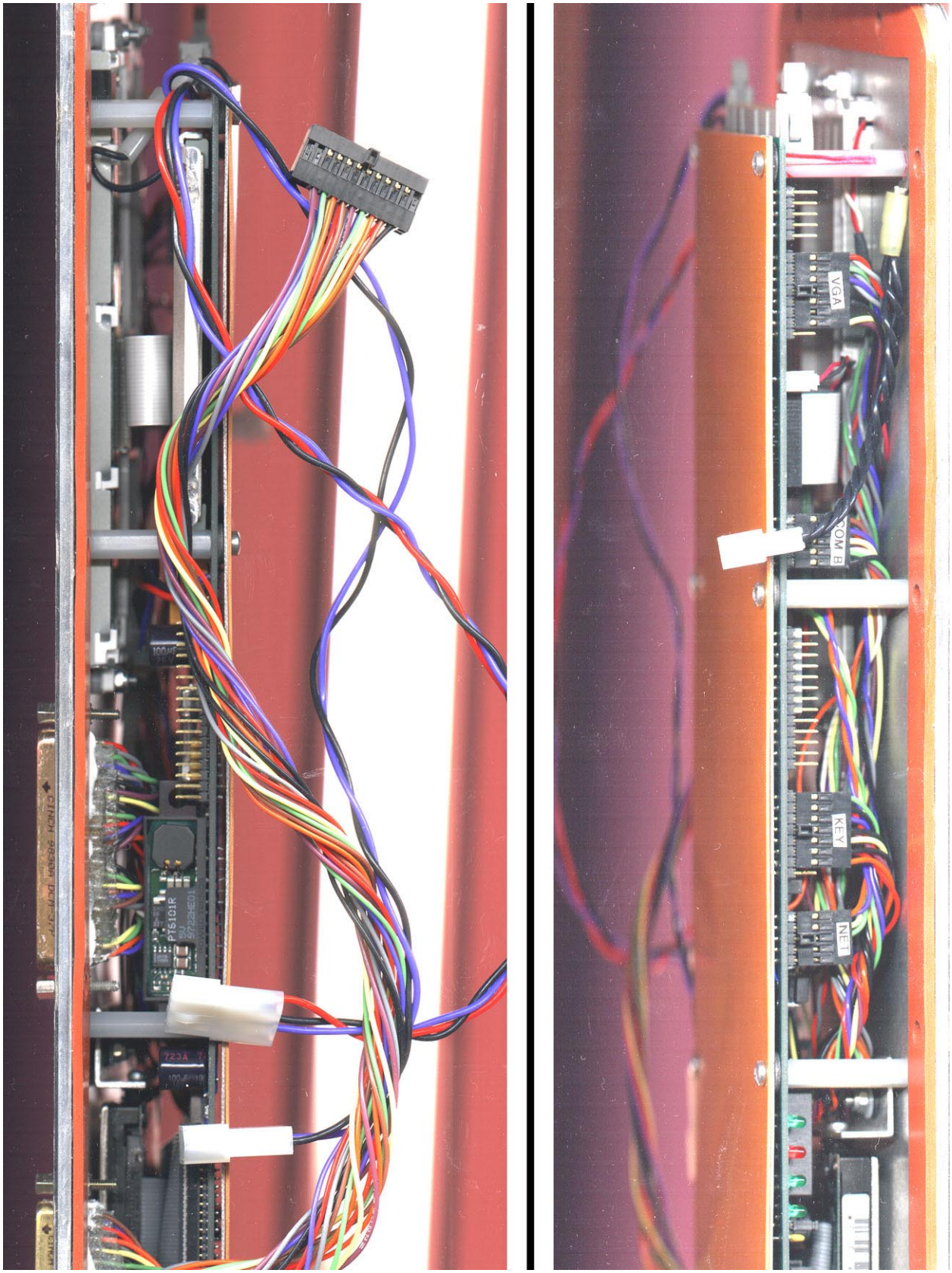

Figure 16.2 - Photo of Front Panel Assembly – (b) Back Side, (c) Front Side

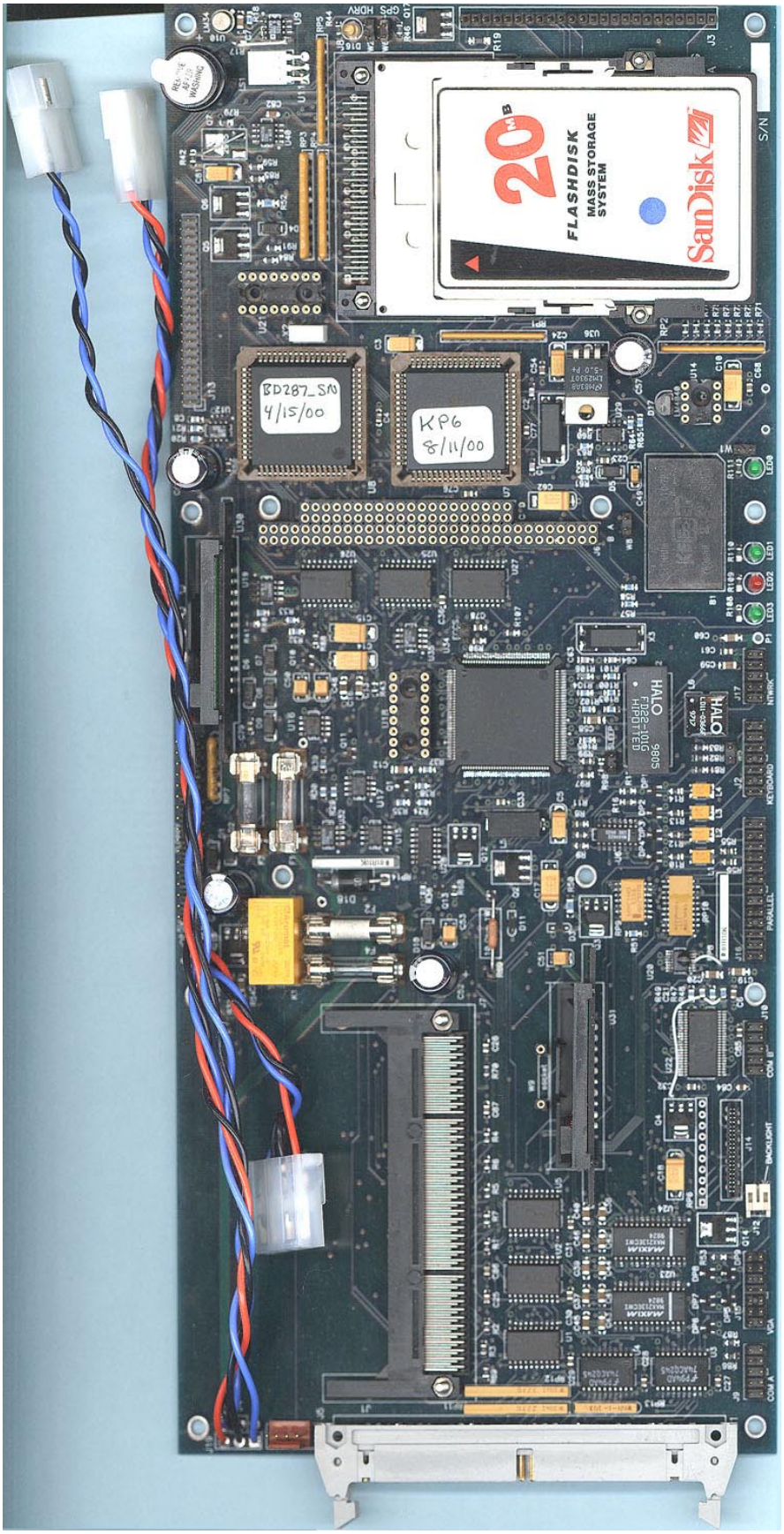

Figure 16.3 – BD287 including the flash disk (top) and the Card PC socket (below)

16.3 CARD-PC MPU BOARD

The AMD 586 Card-PC MPU is mounted on BD287 and is under the LCD display. This board is a self-contained 586 AMD microprocessor operating at 66 MHz. The MPU card contains:

- 1 printer port
- 2 serial ports
- Keyboard / mouse port
- CRT and LCD interfaces
- IDE interface

When configured for the GDP-32^{II}, the Card-PC contains 16 Mb of DRAM. The Card-PC interfaces with peripherals through a single ISA-compatible bus that is used to connect to BD287 discussed below.

16.4 BD287 FRONT PANEL BOARD

The Card-PC MPU module connects directly to BD287 through its EASI bus connector. BD287 is proprietary to Zonge Engineering.

The BD287 board contains:

- All I/O decoding
- Flash disk for program storage, data caches and calibration caches
- keypad decoder
- annunciator
- power monitoring circuits
- power supplies for the digital circuits and LAN interface

The flash disk retains data for extended periods of time even when the GDP-32^{II} is turned off. The capacity of the flash disk is sufficient to hold many days of data under normal use. Time series data obtained while running the AMT/MT program are stored on the hard drive.

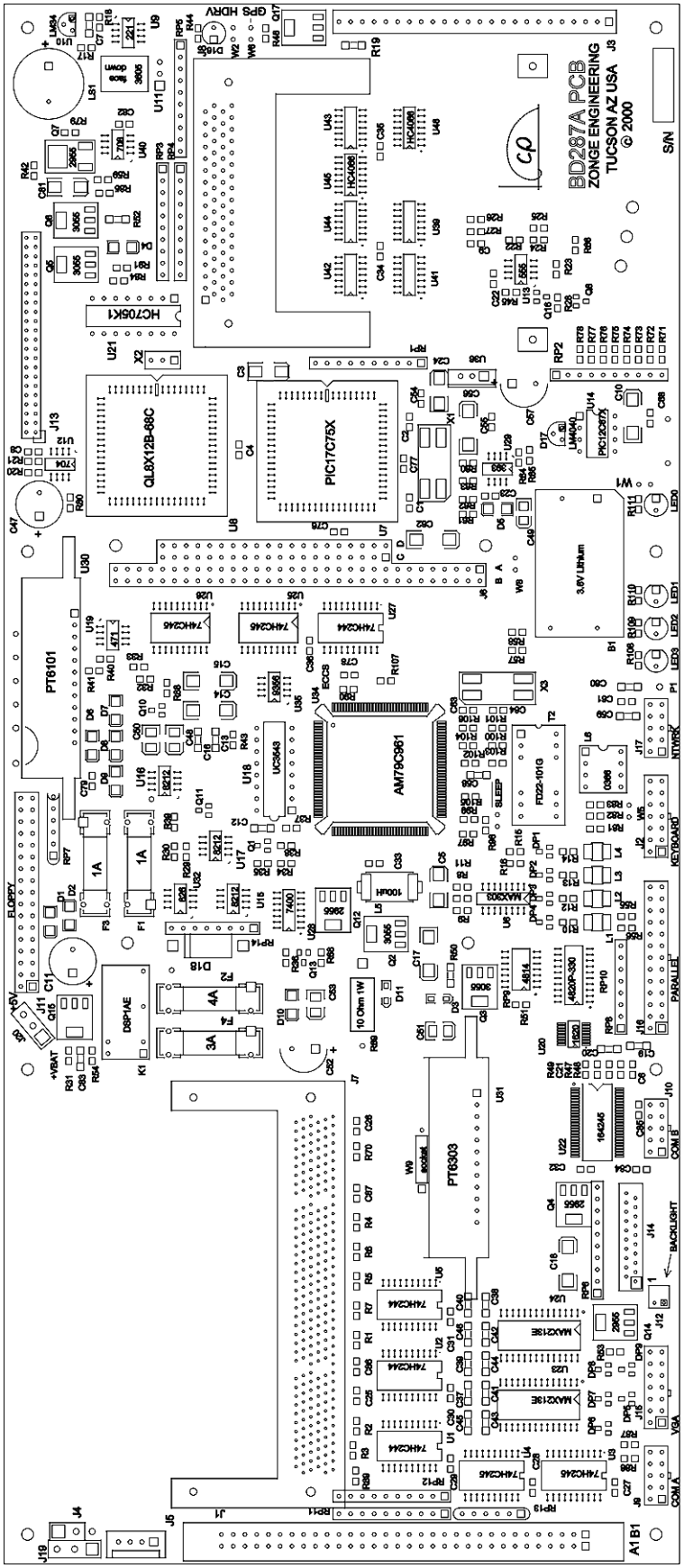

Figure 16.4 - Board diagram of the BD287 Front Panel Board

16.5 BD183 ANALOG BOARD

The small case GDP-32^{II}T has an analog board capacity of 6 channels. The large case GDP-32^{II} has an analog board capacity of 16 channels. The GDP-32^{II} uses one board for each active channel. Boards are installed (up to case capacity) into sequential slots beginning with slot 1, the right-most slot of the analog card cage. .

Each analog board has a number of relay, gain, filter and DAC setting possibilities. Some understanding of the signal path is necessary in order to control the board. The signal path goes through a series of relays to the buffer/differential ***Amplifier Gain*** stage (G0), then to the ***Quad-Notch Filter*** (BP), Amplifier Gain stage (G1), ***Antialias Filter***, Amplifier Gain stage (G2), ***Multiplexer***, and ***ADC*** (see Figure 16.5 (a)).

RELAY FUNCTIONS

There are three input configurations:

1. The Calibrate and Ohmmeter relays are open, permitting measurement of the field signal.
2. The ***Calibrate Relay*** is closed thus providing the Analog Board with a calibrated signal from the Timing/Calibrate Board for self-calibration.
3. Both the ***Ohmmeter*** and Calibrate relays are closed allowing a constant current (100 μa generated on the calibrate board) to flow to the Analog I/O Panel and to the field electrodes. This permits measurement of the electrode contact resistances for each electrode pair.

The ***Attenuator*** relay inserts a resistor attenuator into the signal path to reduce the input signal level by a factor of 0.125.

NOTE: Using the attenuator can cause phase shift at frequencies above 1 kHz due to an increased RC time constant. Since this phase shift is a function of load resistance and cannot be effectively removed, the attenuator is only used at high frequencies when absolutely necessary.

DIFFERENTIAL AMPLIFIER

The input differential amplifier presents a high impedance to the input signal to minimize signal loss and distortion. The differential amplifier combines signals to minimize common mode voltages.

THE OFFSET DAC

The output of a ***Digital-To-Analog Converter*** (DAC) is supplied to each of the BD183 boards. This output offsets any DC signal level (such as SP) appearing on the signal input.

The Digital to Analog Converter (DAC) accepts a digital word from the MPU and produces an analog voltage. The maximum offset value is ±2.5 volts.

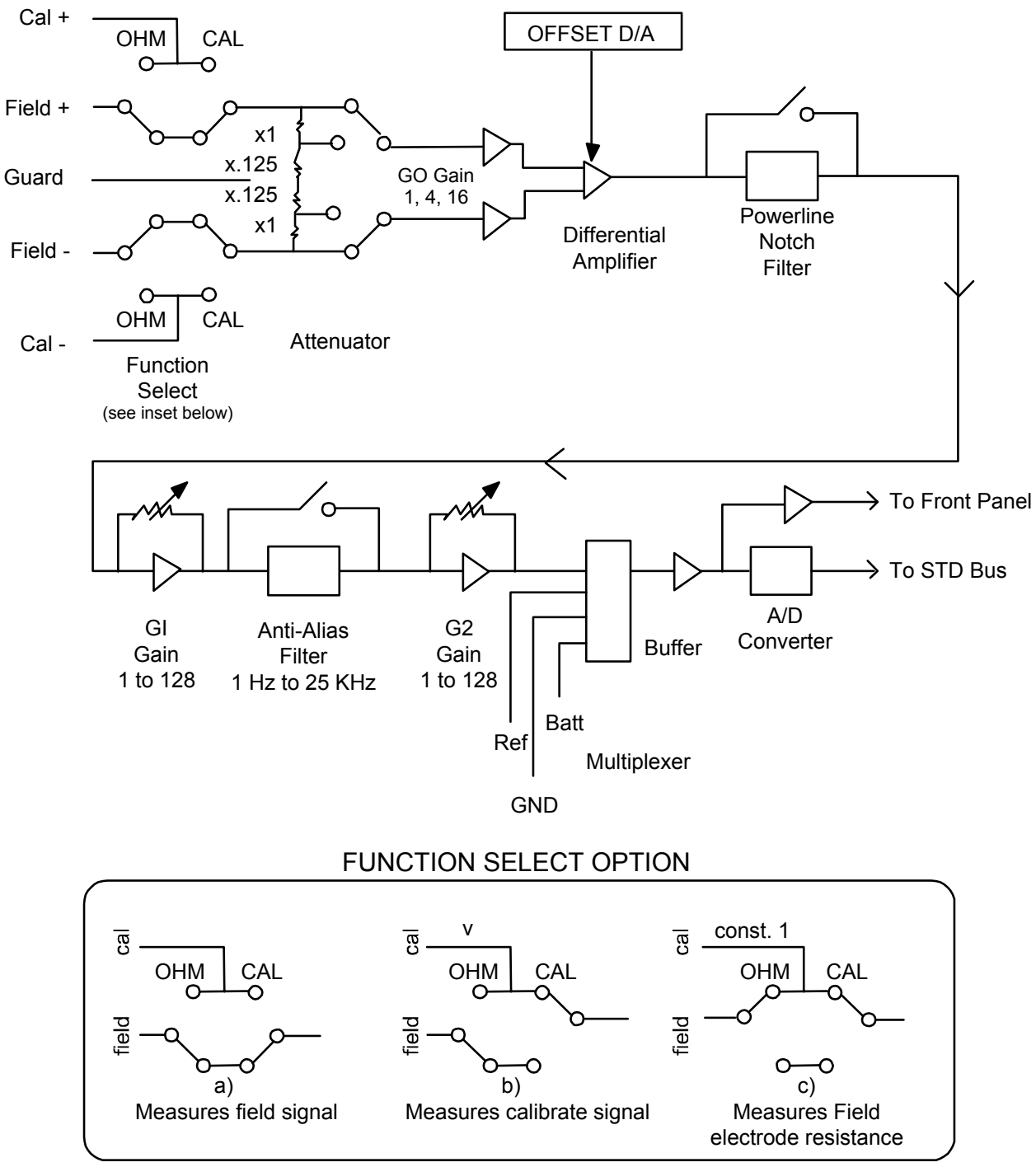

Figure 16.5 (a) - Block Diagram of an Analog Board

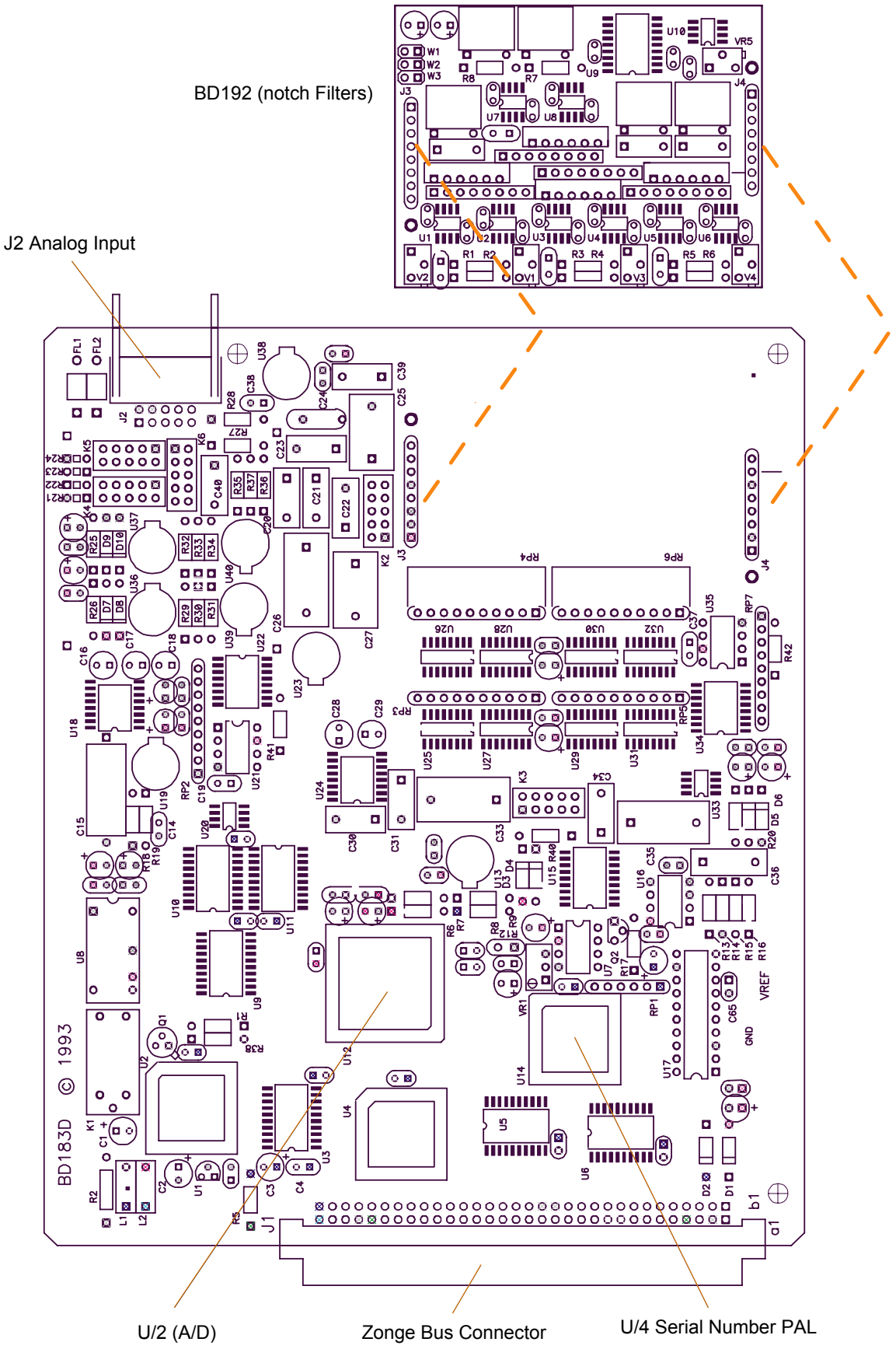

Figure 16.5(b) - Analog Board, BD183D

POWERLINE NOTCH FILTER

The ***Powerline Notch Filter*** can be set to reject the fundamental, 3rd, 5th and 9th harmonics, or any other combination of four harmonic power line frequencies desired.

For example in a country with 50 Hz power mains, the standard filters supplied will reject 50, 150, 250 and 450 Hz. The filters are configured so that you can activate 50 and 150 Hz filters only, or all four simultaneously. The filters may also be bypassed for time-domain applications and for operation in quiet areas. Be aware that use of these filters will cause phase and amplitude distortion around the frequencies of rejection. Such distortion can be removed by calibration with the filters enabled.

GAIN STAGES

Three amplifier gain stages, G0, G1, and G2 provide the signal gain available on the card. G1 and G2 use binary gain steps from 1 to 128 giving a total system gain of 16,384. However, during program operation the gain stages are limited to the range of 1 to 64 each, for a total system gain of 4096. The G0 gain stage is switchable between gains of 1, 4, and 16, for a total maximum gain of 65,536.

ANTI-ALIAS FILTER

This digitally tunable low pass filter is used to attenuate signal frequencies above the desired pass band. Two frequency groups are available and are selected as a LO or HI group. The low group extends from 1 Hz to 255 Hz in 1 Hz increments while the high group extends from 100 Hz to 25.5 kHz in 100 Hz increments. An alias filter bypass is also included for diagnostic testing.

MULTIPLEXER

This stage selects one of four input possibilities and presents the selection to the ADC for conversion. The selections are as follows:

1. **Analog** - The output of the signal amplifiers is provided to the ADC. This is the normal condition.
2. **Reference** - The ADC reference analog voltage is provided to the ADC that normally represents a full-scale count of 32767.
3. **Ground** - Analog ground is connected to the ADC and should result in a 0 count.
4. **Battery** - A voltage of 0.1 times the actual 12-volt battery voltage is presented to the ADC so that the attenuator is not needed. The displayed voltage is multiplied by 10 and thus represents the actual battery voltage.

ANALOG-TO-DIGITAL CONVERTER

The analog-to-digital converter (ADC) converts the received analog signal to a digital format that is stored in computer memory along with other card parameters.

Before the analog voltage signals can be digitally processed, they must first be properly sampled and converted to digital format using an ADC. A 16 bit ADC is used for this purpose on the standard BD183 analog boards. This means that there are 65,536 possible output states on the 16 digital output lines. In the GDP, the states or counts are set up so that 32,767 counts indicates positive full scale voltage, 0 counts indicates zero volts and -32,768 indicates full-scale negative voltage. Full-scale values are determined by the reference voltage (4.5 volts). For example, if an unknown voltage results in 7282 counts, multiply 7282 times 4.5 (reference voltage) and divide by 32767. In equation form the formula for converting digital counts to volts is:

$$volts = \frac{4.5}{32767}\ counts$$

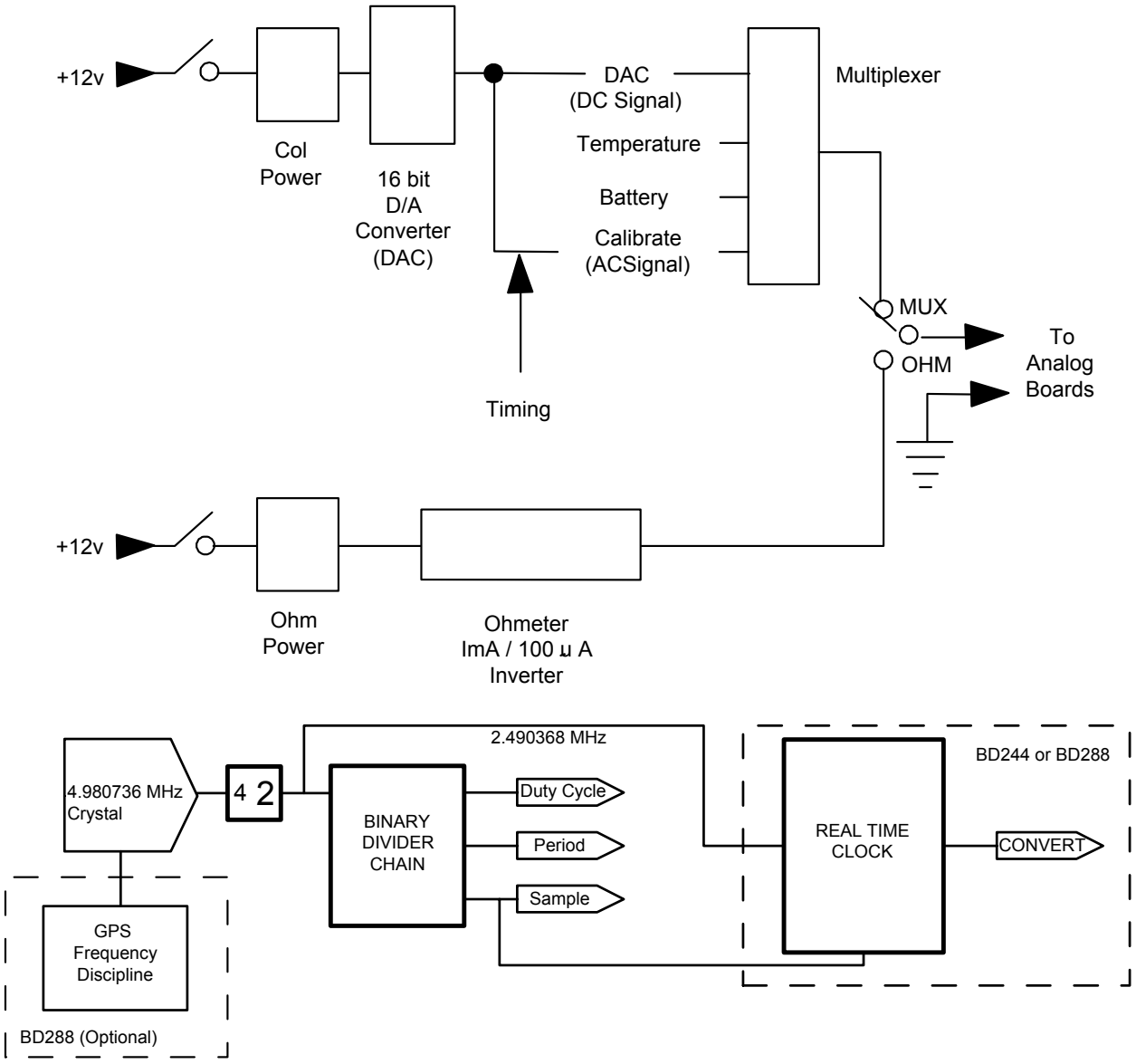

Figure 16.6 (a) – Block Diagram of the Calibrate and Timing Board (BD244 or BD288)

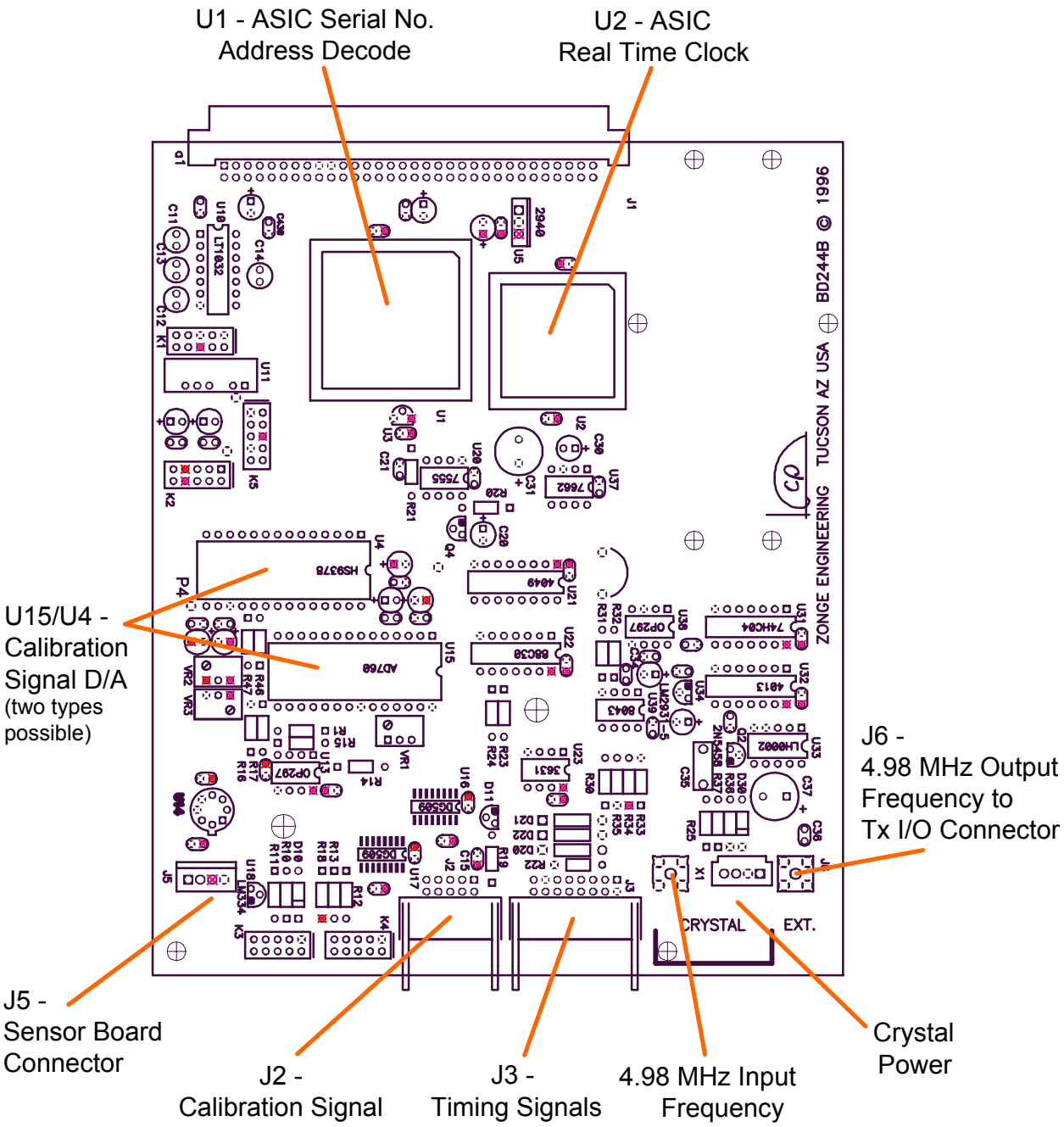

Figure 16.6 (b) - Calibration and Timing Board, BD244

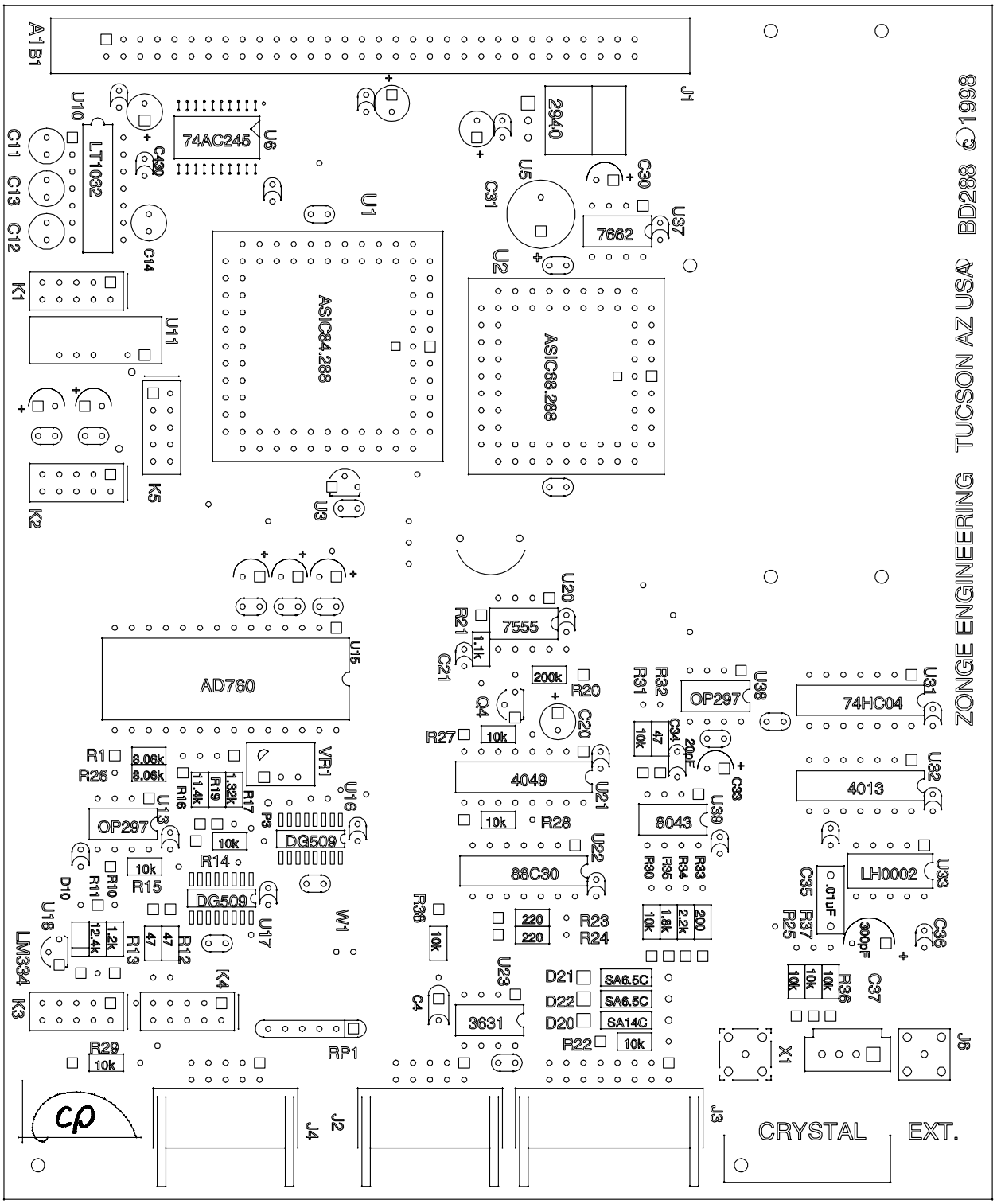

Figure 16.6 (c) - Calibration and Timing Board, BD288

16.6 THE CALIBRATION AND TIMING BOARD

Each GDP-32^{II} receiver contains a Calibration and Timing Board (BD244 or BD288) located in the analog card cage. Figure 16.6 (a) is a simplified block diagram that shows the major functional elements of the board. The three main sections are: Calibrate, Ohmmeter (for checking contact resistance), and Timing.

THE CALIBRATE SECTION AND MULTIPLEXER

The calibration section consists of an AC signal and a DC voltage level from a 16-bit DAC, and temperature and humidity sensors. All of these components are routed to each of the analog channels. Under the control of the GDP-32^{II} software the calibration section supports the following tasks:

- Calibration and/or diagnosis of the analog channels
- Measurement of internal temperature and humidity of the GDP-32^{II}.
- Measurement of electrode resistance

The multiplexer circuit consists of a power supply, a high linearity 16 bit DAC and a four port multiplexer. The power supply on this card and an analog channel must be turned on in order for this circuit to work and the multiplexed output to be read. The multiplexer selects one of four analog signals:

a) **Digital to Analog Converter** (DAC) - The 16 bit DAC on the Calibrate and Timing board generates a DC voltage between -8.35 and +8.35 volts as requested by the digital control signals. Selecting the DAC port provides this level to the system calibration bus. This makes it available to all analog input cards. This DC voltage is used for an accurate system gain calibration.

b) **Calibration** - Selecting this input allows the DAC voltage generated above to be switched at the frequency selected by the timing board, thus generating both a positive and negative signal. The signal generated is either a frequency or time-domain signal as determined by the duty cycle setting on the timing card.

c) **Temperature** - This input is a voltage proportional to internal instrument temperature in °C.

d) **Humidity** - This input is the voltage proportional to internal relative humidity in percent.

OHMMETER

The ohmmeter circuit provides a constant current level to the calibrate bus. An isolated power supply provides power to the ohmmeter. When this relay is turned on, the Calibrate power, if on, is turned off and the Output relay is switched to OHM. The constant current level is selectable at 1.0 ma or 0.1 ma.

TIMING SECTION

The primary function of the timing section is the ***Frequency Generator*** that generates precise timing signals required for the digitization and synchronous detection at 24 binary frequencies ($2^{-10} \leq f \leq 2^{13}$ Hz). There is also a ***Real-Time Clock*** that provides a more accurate time base than the MPU clock.

Frequency Generator

The frequency generator divides the 4.980736 MHz[1] frequency from the master oscillator down into binary frequencies representing the fundamental detection frequencies for the GDP-32^{II} receiver. Corresponding to each of the 24 selectable frequencies, there are 3 relevant synchronous pulse rates:

a) **Period** - A 100% duty cycle pulse rate at the selected frequency.

b) **Duty Cycle** - A 100% duty cycle pulse rate at twice the selected frequency. This frequency is used for the current modulation in time-domain drive and to indicate current ON and current OFF timing for time-domain data acquisition.

c) **Sample** - This pulse frequency provides the ADC convert command that is used for data acquisition at the selected base frequency.

Under control of the MPU, the appropriate frequencies are selected to drive the analog boards, and the transmitter I/O.

Real-Time Clock

A second ASIC has been added to BD244 and BD288, providing a real time clock driven by the 2.490368 MHz frequency. This clock is set by the GDP-32^{II} firmware and thereafter, data are time-stamped with the time kept by BD244/288 rather than the less accurate time kept by the MPU board (running under ROM-DOS). This real-time clock was added to provide an absolute time reference to facilitate obtaining synchronous time-series MT data with multiple receivers, and to enable synchronizing with the GPS system (BD288).

GPS Receiver

A PCI-4 based GPS receiver board can be installed to provide discipline of the 4.980736 MHz crystal. It can also provide for automatic syncing of multiple GDP-32^{II}'s, as well as position information.

[1] The GDP-16 and its predecessor, the GDP-12 were manufactured with 5.0 MHz oscillators, a frequency that cannot be used to generate exact binary frequencies using integer division. Thus, while the frequencies generated are nominally the same, for the purposes of synchronous detection they are different. Because of this the GDP/XMT-32 instruments cannot be used together with earlier generations of the GDP/XMT instrumentation without changing the earlier equipment crystal frequencies from 5.0 MHz to 4.980736 MHz. The crystal oscillator frequency was changed to achieve a significant improvement in noise rejection at the desired detection frequencies.

SMALL CASE

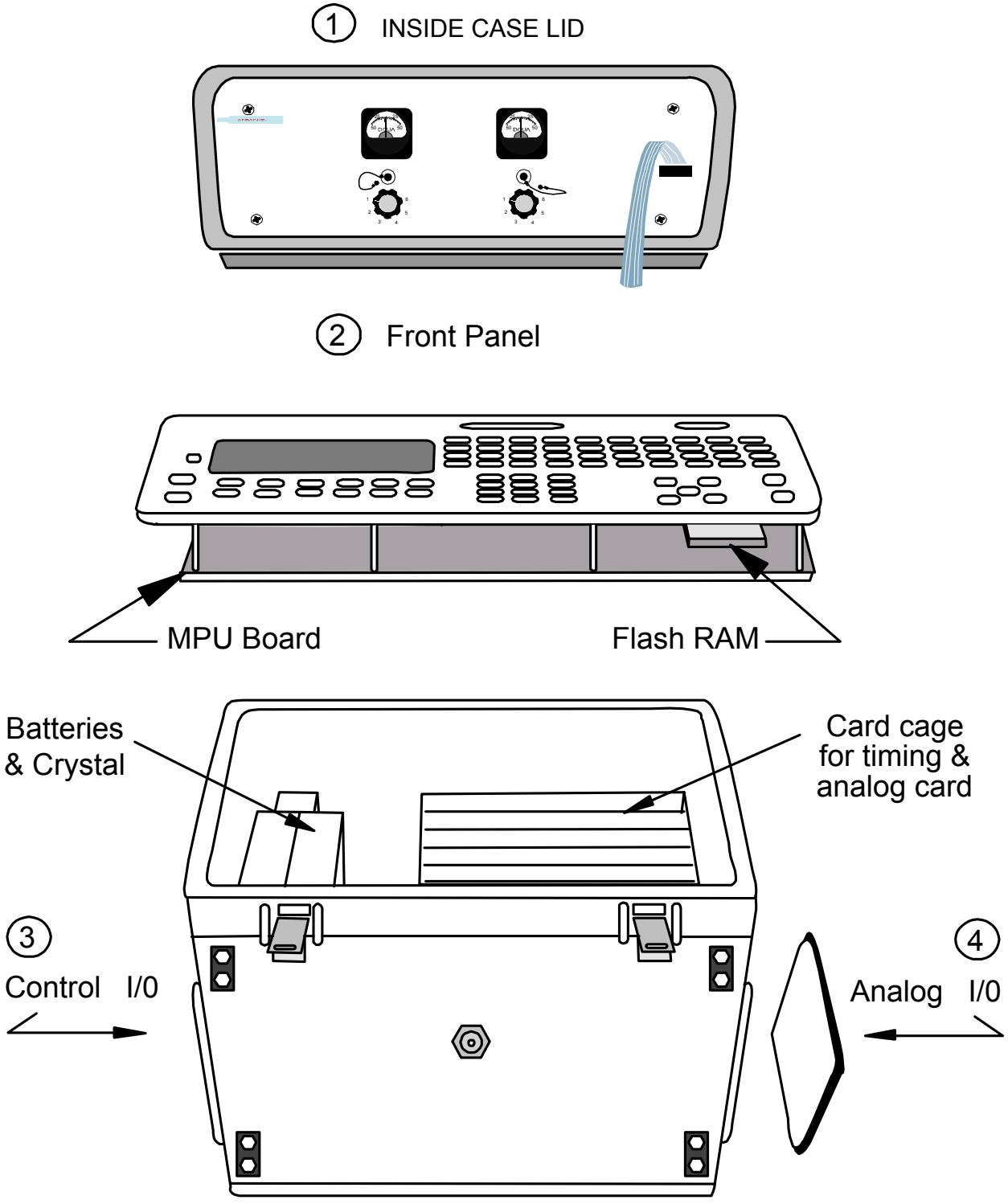

Figure 16.7 - Small Case

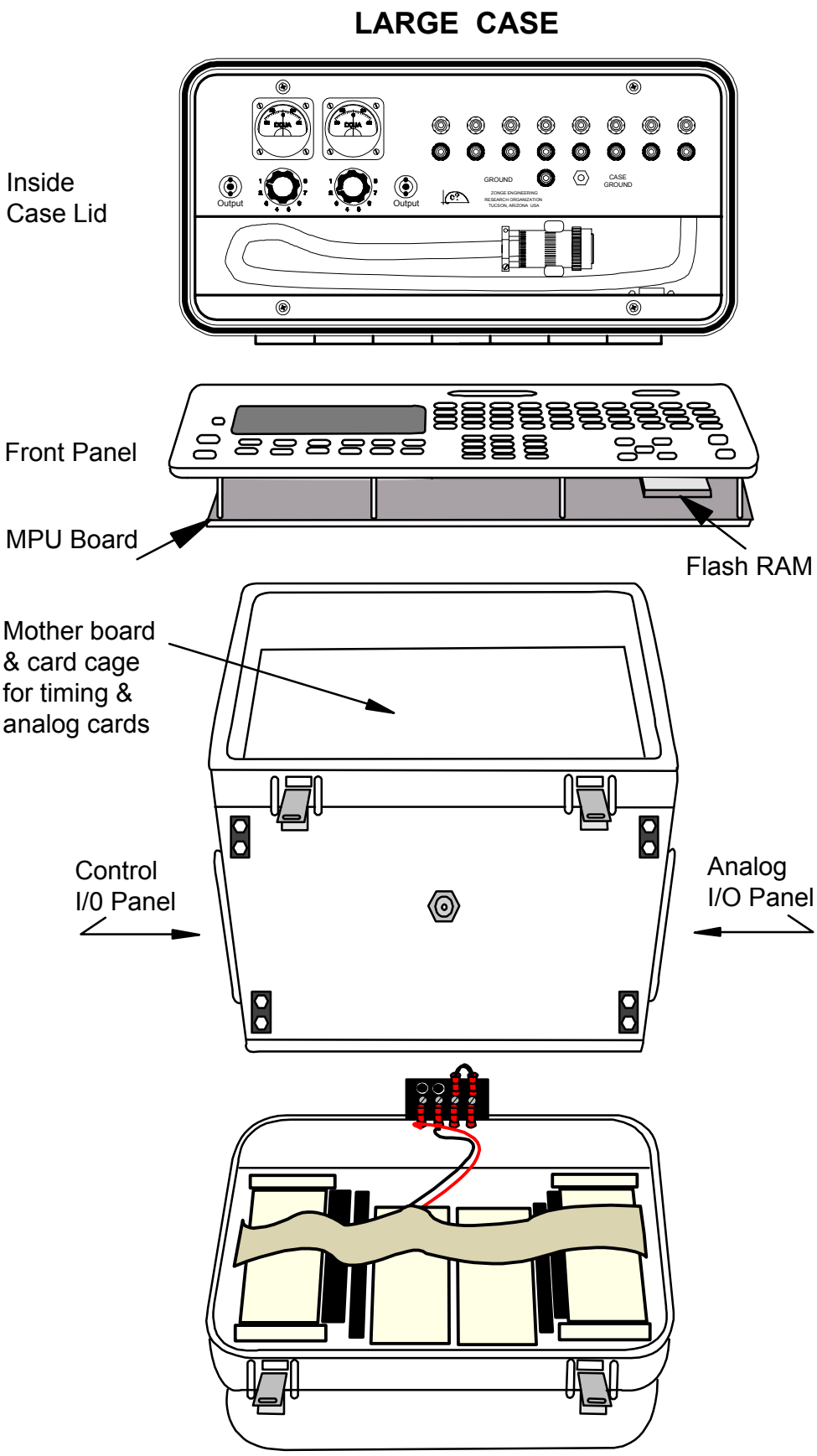

Figure 16.8 (a) - Large Case

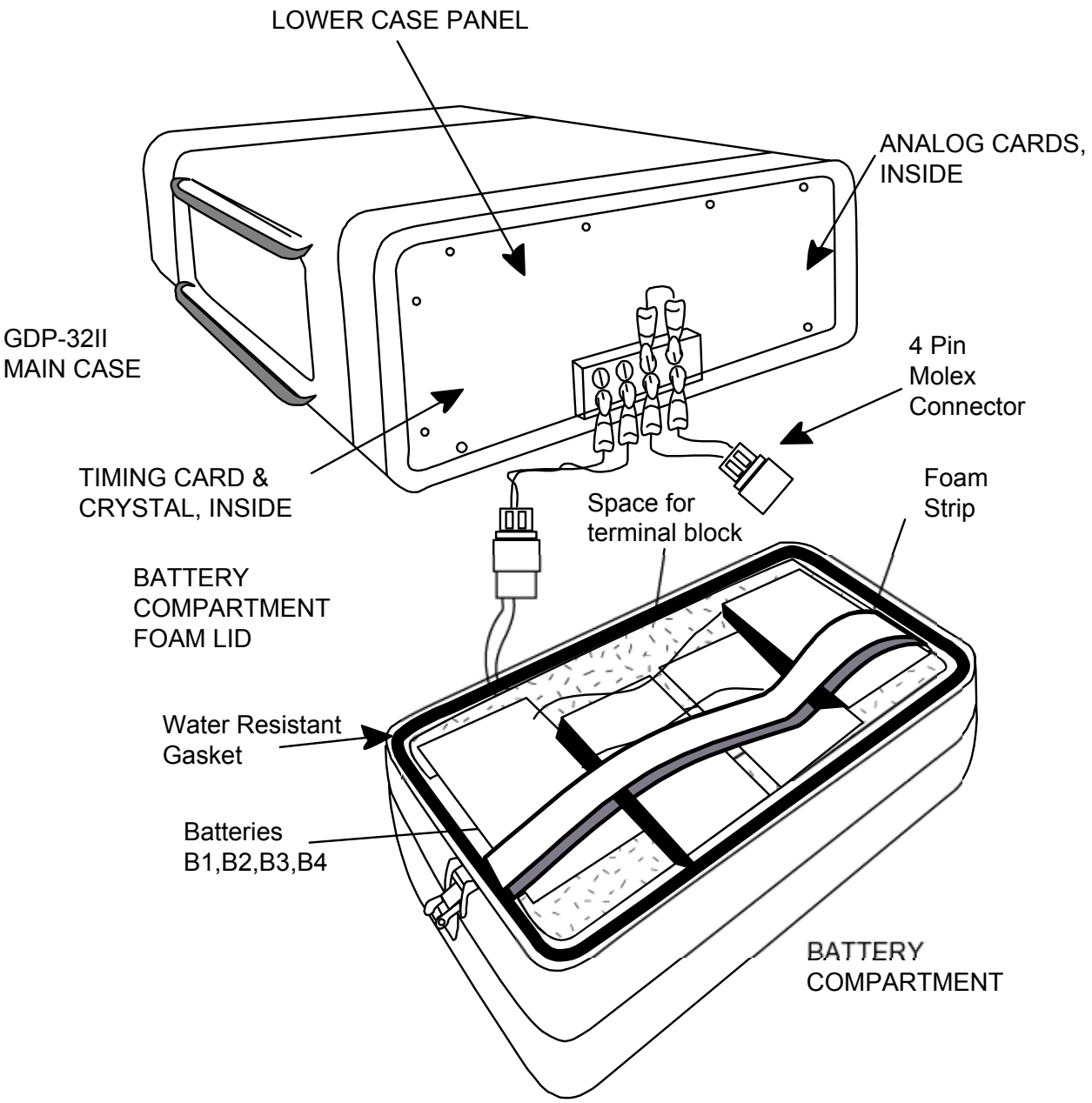

Figure 16.8 (b) - Large Case Battery Compartment

16.7 THE BATTERY COMPARTMENT

SMALL CASE DESIGN (GDP-32^{II}T)

The battery compartment is accessed from the top of the case by removing the front panel. This compartment contains two 6 volt, 10 amp-hour batteries connected in series to provide 12 volts with 10 amp-hours capacity.

To service the battery compartment, remove the front panel assembly and the 4 #6-32 phillips head machine screws that secure the compartment lid to the battery case.

LARGE CASE DESIGN

The battery compartment in the large case GDP-32^{II} connects to the bottom of the receiver case by locking clips. There are four 6 volt batteries, wired in series and parallel to provide a 12 volts with 20 amp-hours capacity.

The Lower Case Panel is removable to permit access to the bottom of the Main Case. There is a 4 amp inline fuse protecting the main 12 v supply. Spare fuses are placed inside the lower case panel in all new GDP-32^{II}s.

Read Section 17.5 before attempting to remove batteries for the large case directly.

NOTE: If one battery goes bad, it is often advisable to replace the complete battery package with new batteries, rather than to replace batteries individually.

A rubber gasket provides a weatherproof seal. Electrical connection is provided through one of two three-wire connectors mounted on the lower case panel. The batteries can be plugged into either connector. The second connector is used to plug in a replacement battery pack before unplugging the battery pack in use, so that power to the timing circuits is not interrupted.

Battery voltage is checked before each data acquisition cycle. It is displayed at the top of the LCD screen. When battery voltage drops below 11.2 volts, a warning message appears, and the operator has 10 to 20 minutes before the circuit breaker disconnects.

Both small and large case models of the GDP-32^{II} contain an electronic circuit breaker located on the front panel board (BD287) that disconnects power when the battery voltage drops below 10.6 volts or rises higher than 15.5 volts.

See Section 17.5 for information on checking and replacing batteries.

16.8 THE CRYSTAL OSCILLATOR

All GDP-32^{II} timing is based on a precision oven-stabilized 4.980736 MHz quartz ***Crystal Oscillator*** *(see footnote on page 16.19)*. The Crystal Oscillator is mounted directly to the calibration and timing board on the large case GDP-32^{II}. On the small case GDP-32^{II}T, it is mounted next to or on top of the battery compartment.

The high accuracy crystal has provisions for both electrical and mechanical trim. Electrical adjustment of the crystal is explained in Section 6.2 and mechanical adjustment is described in Section 17.6.